Power Measurement of NetFPGA Based Router

Feng Guo
School of Electronic Engineering
Dublin City University
Dublin 9, Ireland
feng.guo2@mail.dcu.ie

Olga Ormond
The Rince Institute
Dublin City University
Dublin 9, Ireland
olga.ormond@eeng.dcu.ie

Martin Collier
School of Electronic Engineering
Dublin City University
Dublin 9, Ireland
martin.collier@dcu.ie

Xiaojun Wang
School of Electronic Engineering
Dublin City University
Dublin 9, Ireland
xiaojun.wang@dcu.ie

***Abstract*—As efforts focus towards meeting the EU 20-20-20 targets, energy efficiency in wired networks is a key component not only because of the impact ICT can make in helping the 20% reduction target in greenhouse gases (e.g. replacing flights with video conferences) but also because of the energy savings that network operators can and need to make in running ICT Networks. Especially, as Internet traffic is growing at a fast rate, designing Next Generation Networks (NGN) to be more energy efficient is increasingly important. Approaches towards making network components less energy consuming include: optimising hardware, the use of smart standby and/or adapting the power consumption (by scaling the clock frequency) in response to the traffic load. This paper examines the possible power savings on the NetFPGA 1G reference router when scaling the frequency of router core logic and SRAMs between 125MHz and 62.5MHz. Power measurements taken with the National Instruments USB-6251 for three different packet sizes, are analysed and discussed.**

Keywords- NetFPGA 1G; energy efficiency; frequency scaling

I. INTRODUCTION

Two main drivers that motivate the need of energy efficient Next Generation Networks (NGN) are: regulatory - environment protection, related to decreasing resource wastage and CO2 emissions (by 20% by 2020); and economics, reducing cost mainly for operators (but also for users) in the face of increasing energy prices and increased network traffic, while still maintaining end-to-end Quality of Service (QoS) expected and demanded by users. A huge increase in overall network power consumption is predicted for European ISPs from ~21.4 TWh in 2010to ~35.8 TWh in 2020 if no green technologies are used [1].

Commercial switches and routers on the market today do not include comprehensive energy consumption values. Device specification sheets only report maximum rated power which does not offer an understanding of the actual energy consumption of the networking device. Moreover, most network links and devices are provisioned for busy or rush hour load, which typically exceeds their average utilization. This means that for a large percentage of operation time these links are very over-provisioned.

In order to have a deeper insight into the power consumption of wired network devices, especially for future design, we use the NetFPGA 1G reference router [2]. We explore the impact of various factors such as the processor clock speed, the number of active Ethernet ports, the traffic load, and packet size on the power consumption and performance of the NetFPGA reference router.

In detail, in this paper we examine the impact of :

- Changing the operation frequency of the V3.0.1 NetFPGA board from the higher core logic operation frequency of 125MHz to the lower 62.5MHz operation.
- Changing the number of active ports (from 0 to 4).
- Changing the traffic load (from 0 to 1 Gbps per port).
- Using different packet sizes (140, 531, and 1470 Bytes)

The rest of this paper is organised as follows. Section II describes the NetFPGA 1G reference router. Section III addresses the implementation, describing the testbed used for power consumption data measurements using the National Instruments USB Data Acquisition (DAQ) device. Section IV presents the measurement results and analysis of the NetFPGA1G router power consumption. Section 5 concludes the paper and points out possible directions for future work.

II. NETFPGA 1G REFERENCE ROUTER

The NetFPGA1G board is an open source and low-cost reconfigurable hardware platform optimized as a high-speed networking router. This board is a PCI card that consists of a small Xilinx Spartan II FPGA for the control logic (from PCI interface to the NetFPGA host) and a large Xilinx Virtex-II Pro FPGA for user defined logic programming. The Spartan II works at a fixed frequency, but the Virtex II Pro clock which is the core logic clock can be toggled between 125MHz and 62.5MHz [2]. Two SRAMs run synchronously with the core logic clock also at either 125MHz or 62.5MHz.

In this paper, we used V3.0.1 of the NetFPGA 1G board configured with the reference router (an IPv4 router) [2]. According to the reference router logic, incoming packets go through 5 stages in the packet processing pipeline. Each stage is a separate module. Figure 1 shows these stages: *Stage 1)* the receive queues receive packets from the I/O ports; *Stage 2)* the input arbiter decides which receive queue to service next and takes a packet from that queue and places it in the stage 3 output port lookup; *Stage 3)* the output port lookup decides which port the packet will go out on and then places the packet into the corresponding stage 4 output queue; *Stage 4)* the output queues store packets until the transmit queues are ready to take the packet; *Stage 5)* the transmit queues send the packet out on the corresponding I/O port. The NetFPGA 1G board provides four external network interfaces to the host machine operating system: nf2c0, nf2c1, nf2c2 and nf2c3. The board

itself is connected to the host machine motherboard through a PCI slot. NetFPGA interfaces parameters such as Internet protocol (IP) and media access control (MAC) addresses can be configured using user-level software called SCONE [3]. This software communicates with the NetFPGA 1G board using its corresponding kernel driver.

To use the NetFPGA 1G board as a reference router, the host machine operating system should not be used to configure the board's interface. Otherwise packets from the external interfaces would be hijacked by the host machine operating system. These hijacked packets would pass through the operating system kernel IP stack and update its routing and address resolution protocol (ARP) table ignoring the board routing functionality. For that reason, packets from the host machine should be routed to the NetFPGA interfaces through another network interface existing on the host machine. Thus, the stand alone host machine equipped with a NetFPGA 1G board is only set up to be used as a packet forwarder.

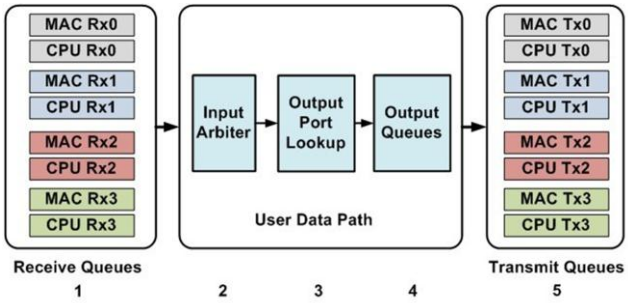

Figure 1. NetFPGA 1G refernce router pipeline

III. IMPLEMENTATION

A. Lab setup

We implemented our lab setup as shown in figure 2. Our setup consists of 2 NetFPGA 1G boards, 3 desktop computers (PCs), an Ultraview PCIEXT-64U [4], and a National Instruments (NI) USB-6251 DAQ [5] for power measurement.

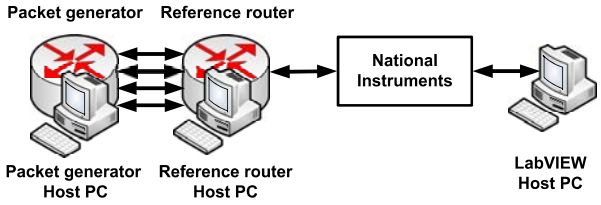

Figure 2. Lab setup

One NetFPGA 1G board is configured as a reference router for receiving and forwarding TCP traffic simultaneously on different ports. The second NetFPGA1G board is setup to run as a packet generator using the Stanford University Packet Generator project [6]. This generator is able to send traffic at any required bitrate. Each of the NetFPGA boards is hosted by a separate PC (installed with CentOS version 5.5). In order to accurately collect power consumption data, there were no other applications running on either of these two NetFPGA host PCs.

One host PC (with Windows 7 installed) is used for the LabVIEW software, which analyses the data from the National Instruments USB DAQ.

B. Power measurement

As shown in figure 3, the tools used for power consumption measurement of the NetFPGA Reference Router in this case are: the Ultraview PCI bus extender PCIEXT-64U, the National Instruments (NI) DAQ USB-6251, and LabVIEW software. The NI USB-6251 is a USB based high-speed data acquisition device which is compatible with LabVIEW 2011 version 11.0 (32-bit) for measuring and capturing power measurement data.

The high speed Ultraview PCI bus extender card is plugged into the motherboard slot of the host PC. This smart bus extender has a 5V, 3.3V and 12V signalling environment. It offers us a way to precisely measure the real-time power consumption of the PCI-based board while the board is working. The power consumption of the NetFPGA 1G reference router can be measured by connecting the white voltage supply pins 3.3V and 5V [7] on the bus extender to the '+' and '-' pins on the NI USB-6251 DAQ device. The NI USB-6251 DAQ is an optimized for superior accuracy at fast sampling rates. It provides a link between the inputs/output signals of the DAQ and the LabVIEW software running on a host PC. The outputs of the 3.3V and 5V voltage supply pins have a one-to-one voltage-to-ampere correspondence. The 12V pin on the bus extender is not used because there is no 12V component on the NetFPGA 1G board.

Finally, LabVIEW software is used to read and collect the power consumption data automatically from the USB DAQ.

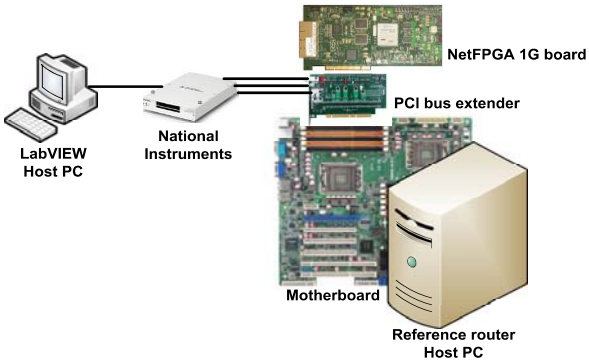

Figure 3. Power measurement

IV. EXPERIMENTS

To examine the power consumption of the NetFPGA 1G reference router running at both 125MHz and at 62.5 MHz, we ran a number of measurement tests: a) **quiescent power measurements** when NetFPGA 1G board is powered up and configured as a router but with no traffic involved; b) **power consumption with different traffic loads** when all the NetFPGA Ethernet ports are active under the same varying traffic load; c) **power consumption for traffic with different packet sizes**. For each test, we have measured 3 million samples and set the sampling rate to 764 KHz, which is the maximum sample rate for the NI USB-6251 DAQ. LabVIEW software is used to automatically calculate and record the average from these 3 million samples.

A. *Quiescent Power*

The Xilinx definition is "Quiescent power (also called static power) is the power drawn by the device when it is powered up, configured with user logic and there is no switching activity". The reference router bitfile is first downloaded into the core Virtex II FPGA so as to configure the NetFPGA 1G board as a hardware-accelerated router. The quiescent power is the power used when this reference router is configured to work as a normal router but with no traffic load activity. In this test, each of four NetFPGA 1G Ethernet ports is activated in turn and the power consumption is measured for both 125MHz and 62.5MHz. As shown in table I, the difference of average quiescent power of NetFPGA 1G router working between 125MH and 62.5MHz is on average 1.14W. This 1.14W power difference is mainly from the consumption in core VirtexII FPGA and the SRAMs operating.

TABLE I. QUISCIENT POWER CONSUMPTION VERSES NUMBER OF ACTIVE PORTS

No. of Active Ports	Power Consumption (Watt)	
	125MHz	*62.5MHz*
0	6.747672	5.525770
1	7.581619	6.447695
2	8.572116	7.426604
3	9.592518	8.459156
4	10.610967	9.544976

As noted earlier, these results were obtained using V3.0.1 software release for the NetFPGA 1G. They differ in some respects from earlier measurements of quiescent power documented in [8], which were obtained on V2.2.0 of the NetFPGA software release. The latter figures are higher for 125MHz operation and lower for 62.5MHz operation. Thus the effect of frequency scaling is more pronounced when using V2.2.0 (with a difference in average consumption of 1.98W vs 1.14W). This will be discussed further in section V.

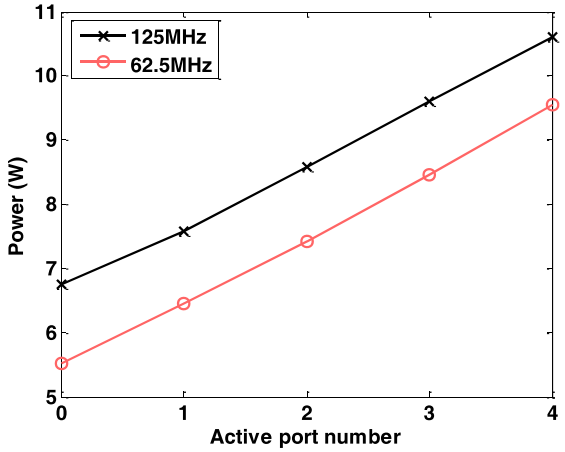

Figure 4. Power consumption under different number of active ports

As shown in figure 4, power consumption increases linearly with the number of active ports on the NetFPGA router. Activating each port leads to around 1W extra power consumption. Operations of PHY and MAC components such as enabling the link and implementing the carrier sensing would result in this linear increase.

B. *Varying Load and Packet Size Power*

This experiment aims to measure the power consumption of the NetFPGA 1G reference router while in operation as a router forwarding traffic on all the four interfaces. The NetFPGA 1G packet generator was used to generate 10 different aggregate input traffic loads (400Mbps, 800Mbps, 1200Mbps, 1600Mbps, 2000Mbps, 2400Mbps, 2800Mbps, 3200Mbps, 3600Mbps and 4Gbps) and with 3 different packet sizes (140Byte, 531Byte and 1470Byte).

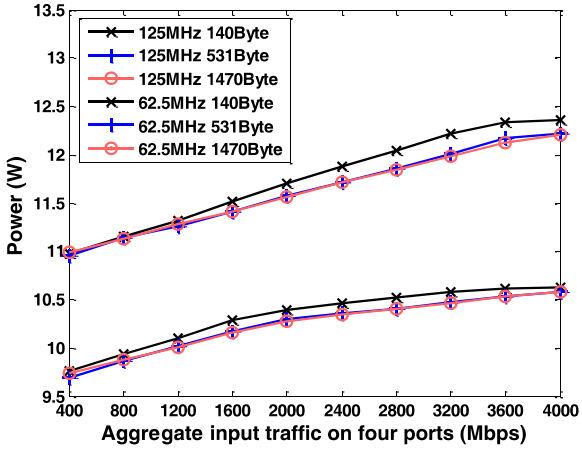

Figure 5. Power consumption for varying input load and varing packet size at both frequencies

The power consumption measurements taken are shown in figure 5. It can be clearly seen that more power is consumed by the board when it works at the higher (125MHz) frequency. Power consumption also increases with increase in traffic load.

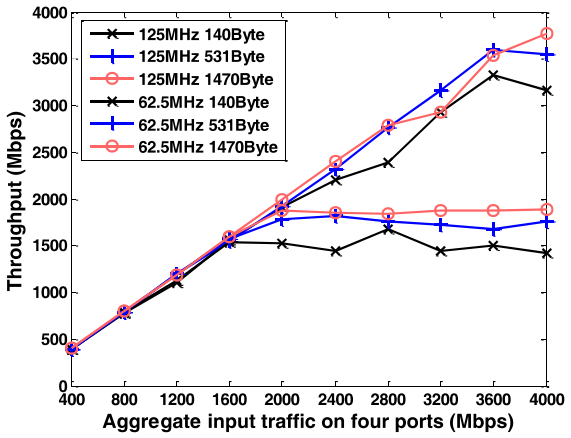

Figure 6. Throughput for varying input load and varying packet size at both frequencies

The NetFPGA 1G router provides its maximum 4 Gbps speed routing when the core Virtex II FPGA is running at 125MHz. Theoretically, the throughput of the NetFPGA 1G router should degrade to approximately half if we scale down the core Virtex II FPGA frequency by half (from 125MHz to 62.5MHz). Thus the NetFPGA 1G router should only provide a maximum processing speed of 2Gbps when the core Virtex II FPGA is running at 62.5MHz. As shown in figure 6, as

expected, the throughput is all below 2Gbps for 62.5MHz even for aggregate input traffic loads that are above 2Gbps.

Results also show the difference that packet size plays on the power consumption. We can notice that the smaller packets (140 Byte) have a higher power consumption and lower throughput than either the 531 or 1470 Byte packets, this may be attributed to the fact that there is more packet header processing required per byte of payload for smaller packet sizes.

As shown in figure 7, when the NetFPGA 1G router is operating at the lower frequency (62.5MHz), the router cannot handle traffic loads greater than 2Gbps. There is very visible performance degradation in terms of unacceptable packet loss rate for input rates above this threshold. The packet loss for 125MHz is relatively acceptable: 0 in most cases for the lower input rates with packet loss starting at 865 Mbps for 140 byte packets, 917 Mbps for 531 byte packets, and 954 Mbps for 1470 byte packets. Again the smaller packets suffer greater packet loss at the higher loads than the larger packets, which again we attribute to the need for more packet header processing per byte of payload required for the smaller packets.

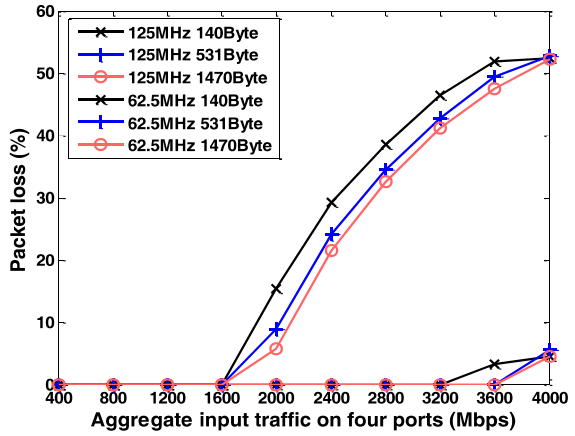

Figure 7. Packet loss for varying input load and varying packet size at both frequencies

TABLE II. POWER CONSUMPTION OF NETFPGA 1G REFERENCE ROUTER

Input Traffic (4 Ports Active)	Power Consumption(Watt)					
	140Byte		*531Byte*		*1470Byte*	
	125MHz	*62.5MHz*	*125MHz*	*62.5MHz*	*125MHz*	*62.5MHz*
0Mbps	10.6109	9.5449	10.6109	9.5449	10.6109	9.5449
400Mbps	10.9788	9.7586	10.9596	9.6969	10.9866	9.7340
800Mbps	11.1575	9.9409	11.1407	9.8690	11.1333	9.8793
1200Mbps	11.3166	10.0971	11.2634	10.0246	11.2785	10.0137
1600Mbps	11.5231	10.2949	11.4173	10.1774	11.4167	10.1627
2000Mbps	11.7063	10.3910	11.5704	10.2972	11.5656	10.2753
2400Mbps	11.8833	10.4666	11.7116	10.3648	11.7116	10.3468
2800Mbps	12.0389	10.5176	11.8600	10.4111	11.8487	10.4111
3200Mbps	12.2219	10.5777	12.0102	10.4803	11.9907	10.4673
3600Mbps	12.3410	10.6197	12.1681	10.5374	12.1273	10.5292
4Gbps	12.3568	10.6330	12.2239	10.5852	12.2088	10.5796

V. CONCLUSIONS

The results from our power measurements show that:

- The NetFPGA 1G reference router power consumption increases linearly with the number of active ports (0-4). ~1W per port.
- The NetFPGA 1G reference router consumes proportional energy to its traffic load.
- For the NetFPGA 1G reference router, larger packet sizes means less power consumption, less packet loss and higher throughput per byte of payload.
- Deactivating ports, rerouting and aggregating traffic may be the most efficient means for power savings for wired routers, rather than leaving all the ports on with a low traffic load.
- Frequency scaling can be considered as an add-on feature for extra small power savings. Considering lighter aggregate traffic loads of <1600Mbps, scaling down the frequency from 125MHz to 62.5MHz would save 1.3 W without impacting the end-to-end QoS.

The results for quiescent power consumption documented here and in [8] indicate that the energy saving consequent upon switching to a lower frequency is less pronounced in the newer 3.0.1 version of the NetFPGA software. We are currently studying the relevant Verilog code to determine the mechanism underlying this behaviour.

ACKNOWLEDGMENT

This work was co-funded by the FP7 ECONET project and the China Scholarship Council. Thanks also to Jean-Dominique Innocenti, Leonardo Fialho, Tom Molloy, and our collaborators in Lightcom for their assistance in the power measurements.

REFERENCES

[1] Global e-Sustainibility Initiative (GeSI), "SMART 2020:Enabling the Low Carbon Economy in the Information Age", http://www.theclimategroup.org/assets/resources/publications/Smart2020Report.pdf.

[2] Gibb, G., Lockwood, J. W., Naous, J., Naous, J., Hartke, P., McKeown, N. NetFPGA -- Open Platform for Teaching How to Build Gigabit-rate Network Switches and Routers. In *IEEE Transactions on Education*,Vol. 51, No. 3, Aug. 2008. http://netfpga.org/foswiki/bin/view/NetFPGA/OneGig/ReferenceRouterWalkthrough

[3] Stanford University, NetFPGA SCONE Homepage. http://netfpga.org/foswiki/bin/view/NetFPGA/OneGig/SCONEWalkthrough.

[4] Ultraview PCI bus extender. http://ultraviewcorp.com/displayproduct.php?part_id=4&sub_id=2.

[5] National Instruments USB-6251 DAQ Device http://sine.ni.com/nips/cds/view/p/lang/en/nid/202802

[6] Covington, G. Gibb, G., Lockwood, J.W., Mckeown, N. "A Packet Generator on the NetFPGA Platform," *Field Programmable Custom Computing Machines, 2009. FCCM '09. 17th IEEE Symposium on,* 235-238, Apr. 2009.

[7] Sivaraman, V., Vishwanath, A., Zhao, Z. and Russell, C. Profiling per-packet and per-byte energy consumption in the NetFPGA Gigabit router. In *Computer Communications Workshops (INFOCOM WKSHPS), 2011 IEEE Conference on*,331- 336, Apr. 2011.

[8] Guo, F., Olga, O., Fialho, L., Collier, M., and Wang. X. Power consumption analysis of a NetFPGA based router. *The Journal of China Universities of Posts and Telecommunications.(* in press).